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Date of mailing (day/month/year) 04 December 2000 (04.12.00)	
International application No. PCT/IB00/00536	**Applicant's or agent's file reference** P8017.WO
International filing date (day/month/year) 27 April 2000 (27.04.00)	**Priority date** (day/month/year) 30 April 1999 (30.04.99)
Applicant O'FARRELL, Timothy et al	

1. The designated Office is hereby notified of its election made:

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10/009657
Rec'd PCT/PTO 30 OCT 2001
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ART 34 AMDT

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DATA COMMUNICATION IN A WIRLESS LOCAL AREA NETWORK USING M-ARY CODE KEYING

The present invention relates to data communication and more particularly, to data communication using spread spectrum techniques. The invention also relates to communication applications using signature sequences.

Spread spectrum communication techniques are used for information carrying signals in a variety of communication systems because of their ability to reduce the effects of certain transmission impairments. Many multi-user communication techniques suffer co-channel interference, multiple access interference and intersymbol interference. The use of spread spectrum transmission and reception attenuates these interference types.

In Local Area Networks (LANs) there is an increasing need for wireless access. This wireless access allows mobile computer users to remain in contact with a given corporate LAN over short distances. Currently available systems provide such connections using either radio or infrared communication technology. For certain system requirements, this communication is adequate. However, the data transmission rates achievable are relatively low and this significantly limits the number of applications to which the systems may be applied and implementation costs are often prohibitive.

Wireless local area network (WLAN) products were thus for a long time a specialty, made available by a small number of vendors and built accordingly to meet proprietary requirements. The Institute of Electrical and Electronic Engineers (IEEE) in June 1997 formalized a standard that will control interoperability of such products known as 802.11. While this standard will undoubtedly promote the growth of WLAN products, the problems of transmission rates, reliability and cost remain. One possible solution is obtained by the application of spread spectrum communication techniques using signature sequences. One such approach is identified in "A 2.4GHz 11 MBps Baseband Processor for B02.11 Applications", ANDREN; Harris Semiconductor (05-05-1998). While implementations of this type overcome the traditional problems, it is difficult to synchronise data communication

without the use of complex circuitry. Synchronisation difficulties include chip and symbol synchronisation as well as the problem of signal strength measurement.

One solution to these problems has been proposed by Harris (i.e. the Intersil PRISM radio chip set) for use in the new 802.11 WLAN standard at 11 Mb/s. In common with most proposed solutions there is a phase involving the acquisition of synchronisation and a phase involving the maintenance. Acquisition in this case, is accomplished using a single correlator and an embedded Barker sequence. Synchronisation is maintained using an early-late detector. See "A 156 – MB/S Interface CMOS LSI for ATM Switching Systems", KOZAKI T. *et al* Ieice Transactions on Communications, JP, Institute of Electronics Information and Communication Engineering, Tokyo (01-06-1993), E76-B (6), 684-693. While the previously known 'Harris type' early-late detector solution is practical in a wide variety of applications, the early-late detector operates directly on the incoming sequence stream, which is composed of binary codes at the input. This leads to reliability problems in that quality of the signal cannot be guaranteed.

There is therefore a need for a method and apparatus, which will overcome the aforementioned problems.

It is an object of this invention to provide a method and apparatus for data communication which delivers synchronisation acquisition in terms of chip and symbol synchronisation and signal strength measurement (SSM).

It is a further object of the invention to provide synchronisation maintenance in terms of chip synchronisation.

Accordingly there is provided a method and apparatus for data communication in a WLAN network using M-ary Code Keying.

Preferably M-ary Code Keying is used for synchronisation of data communication in the network.

Preferably the synchronisation scheme utilises Supergold Structured Codes for acquisition. These codes are described in WO99/33212.

Ideally, the synchronisation scheme also utilises Supergold Structured Codes for maintenance.

It will also be understood that the method and apparatus described may be used in any suitable communication medium

It will be noted that the method and apparatus is not limited to implementation with the packet based IEEE 802.11 standard but may equally be implemented with any packet based transmission scheme as well as for synchronous transmission with embedded synchronisation symbols.

It will of course be understood that the present invention is not limited to the specific details described herein, which are given by way of example only and that various modifications and alterations are possible within the scope of the invention as defined by the appended claims.

CLAIMS

1. A method for data communication in a Wireless local area network (WLAN) using a plurality of correlators and M-ary Code Keying with an associated chip period characterised in that the communication utilises a signature sequence of the type generated by performing the steps of

    selecting a seed set of sequences of a given size having a plurality of inner sequences,

    generating a plurality of cosets from the seed set of sequences by multiplying in turn each inner sequence by an element of an associated sequence,

    constructing a subset of sequences by concatenating the sequences of a coset and

    constructing a full set of sequences by concatenating subsets of sequences,

    for simultaneously generating:-

    a periodic signal for acquiring symbol synchronisation; and

    a difference squarewave signal for acquiring and maintaining chip synchronisation, a chip synchronisation signal being generated by subtracting the sum of even groups of correlator outputs from the sum of odd groups of correlator outputs.

2. A method as claimed in claim 1 in which the utilisation of the signature sequence further generates a sum signal for determining received signal strength and setting threshold levels.

3. A method as claimed in claim 1 or 2 in which the sum of the responses of all correlators to the repetitive periodic transmission of one code is a constant.

4. A method as claimed in any preceding claim in which the difference signal is a periodic bipolar squarewave signal.

5. A method as claimed in claim 4 in which the periodic bipolar squarewave signal has a period of twice the chip period.

6. A method as claimed in any preceding claim including the step of generating a periodic transmission for producing a zero value sidelobe of a summed correlation.

7. A method as claimed in claim 6 in which summation of the correlators is initiated in response to the periodic transmission.

8. A method as claimed in claim 7 in which the correlator summation is directed to a thresholding circuit.

9. A method as claimed in claim 7 or claim 8 in which the correlator summation is directed to a comparison logic for level determination.

10. A method as claimed in any preceding claim in which an early-late detector circuit is connected at the correlator outputs.

11. A method as claimed in claim 10 incorporating means for window-thresholding a chip synchronisation waveform.

12. A data communications apparatus for use in a Wireless local area network (WLAN) incorporating a plurality of correlators and being formed for M-ary Code Keying at an associated chip period characterised in that the apparatus is formed for communication with a signature sequence of the type generated by;

means for selecting a seed set of sequences of a given size having a plurality of inner sequences,

means for generating a plurality of cosets from the seed set of sequences by multiplying in turn each inner sequence by an element of an associated sequence,

means for constructing a subset of sequences by concatenating the sequences of a coset,

means for constructing a full set of sequences by concatenating subsets of sequences,

means for generating a periodic signal for acquiring symbol synchronisation; and

means for generating a difference squarewave signal for acquiring and maintaining chip synchronisation and for generating a chip synchronisation signal by subtracting the sum of even groups of correlator outputs from the sum of odd groups of correlator outputs.

13. An apparatus as claimed in claim 12 incorporating means for generating a sum signal for determining received signal strength and setting threshold levels.

14. An apparatus as claimed in claim 12 or 13 in which the sum of the responses of all correlators to the repetitive periodic transmission of one code is a constant.

15. An apparatus as claimed in any of claims 12 to 14 in which the difference signal is a periodic bipolar squarewave signal.

16. An apparatus as claimed in claim 15 in which the periodic bipolar squarewave signal has a period of twice the chip period.

17. An apparatus as claimed in any of claims 12 to 16 incorporating periodic transmission means for producing a zero value sidelobe of a summed correlation.

18. An apparatus as claimed in claim 17 in which summation of the correlators is initiated in response to the periodic transmission.

19. An apparatus as claimed in claim 18 in which the correlator summation is directed to a thresholding circuit.

20. An apparatus as claimed in claim 18 or claim 19 in which the correlator summation is directed to a comparison logic for level determination.

21. An apparatus as claimed in any of claims 12 to 20 in which an early-late detector circuit is connected at the correlator outputs.

22. An apparatus as claimed in claim 21 incorporating means for window-thresholding a chip synchronisation waveform.

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WORLD INTELLECTUAL PROPERTY ORGANIZATION
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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 7 : H04B 1/707

A1

(11) International Publication Number: WO 00/67388

(43) International Publication Date: 9 November 2000 (09.11.00)

(21) International Application Number: PCT/IB00/00536

(22) International Filing Date: 27 April 2000 (27.04.00)

(30) Priority Data:
S990361 30 April 1999 (30.04.99) IE

30 Oct 01 / 30mos

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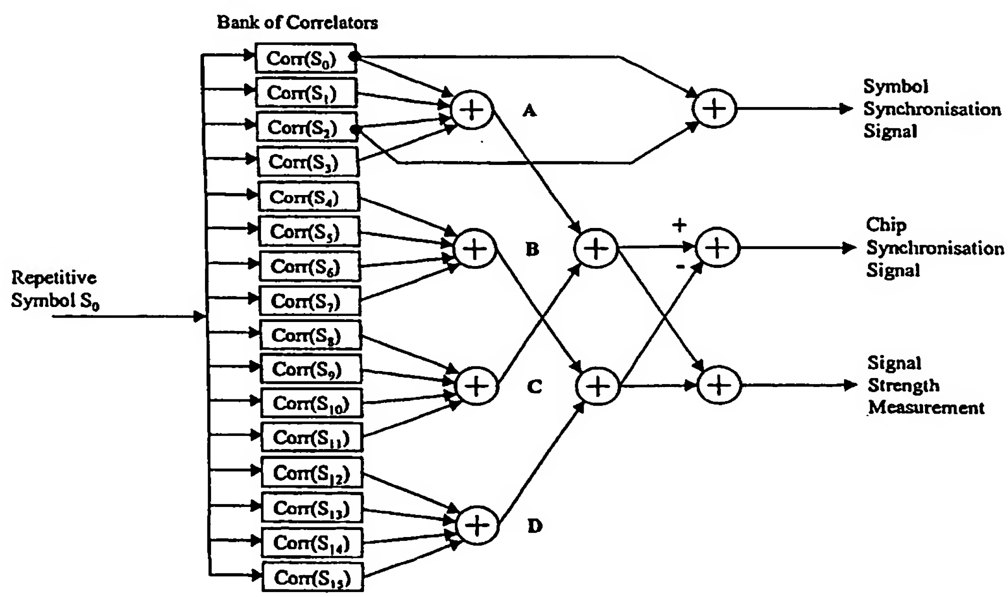
(81) Designated States: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published

With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: DATA COMMUNICATION IN A WIRELESS LOCAL AREA NETWORK USING M-ARY CODE KEYING



(57) Abstract

A method and apparatus for data communication using signature sequences and spread spectrum techniques to reduce the effects of certain transmission impairments in a Wireless local area network (WLAN). The invention uses a number of correlators and M-ary Code Keying with a Supergold signature sequence for simultaneously generating a periodic signal for acquiring symbol synchronisation, a difference squarewave signal for acquiring and maintaining chip synchronisation and a sum signal for determining received signal strength and setting threshold levels.

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DATA COMMUNICATION IN A WIRELESS LOCAL AREA NETWORK USING M-ARY CODE KEYING

The present invention relates to data communication and more particularly, to data communication using spread spectrum techniques. The invention also relates to communication applications using signature sequences.

Spread spectrum communication techniques are used for information carrying signals in a variety of communication systems because of their ability to reduce the effects of certain transmission impairments. Many multi-user communication techniques suffer co-channel interference, multiple access interference and intersymbol interference. The use of spread spectrum transmission and reception attenuates these interference types.

In Local Area Networks (LANs) there is an increasing need for wireless access. This wireless access allows mobile computer users to remain in contact with a given corporate LAN over short distances. Currently available systems provide such connections using either radio or infrared communication technology. For certain system requirements, this communication is adequate. However, the data transmission rates achievable are relatively low and this significantly limits the number of applications to which the systems may be applied and implementation costs are often prohibitive.

Wireless local area network (WLAN) products were thus for a long time a specialty, made available by a small number of vendors and built accordingly to meet proprietary requirements. The Institute of Electrical and Electronic Engineers (IEEE) in June 1997 formalized a standard that will control interoperability of such products known as 802.11. While this standard will undoubtedly promote the growth of WLAN products, the problems of transmission rates, reliability and cost remain. One possible solution is obtained by the application of spread spectrum communication techniques using signature sequences. While implementations of this type overcome the traditional problems, it is difficult to synchronise data communication without the use of complex circuitry. Synchronisation difficulties include chip and symbol synchronisation as well as the problem of signal strength measurement.

One solution to these problems has been proposed by Harris (i.e. the Intersil PRISM radio chip set) for use in the new 802.11 WLAN standard at 11 Mb/s. In common with most proposed solutions there is a phase involving the acquisition of synchronisation and a phase involving the maintenance. Acquisition in this case, is accomplished using a single correlator and an embedded Barker sequence. Synchronisation is maintained using an early-late detector. While the previously known 'Harris type' early-late detector solution is practical in a wide variety of applications, the early-late detector operates directly on the incoming sequence stream, which is composed of binary codes at the input. This leads to reliability problems in that quality of the signal cannot be guaranteed.

There is therefore a need for a method and apparatus, which will overcome the aforementioned problems.

It is an object of this invention to provide a method and apparatus for data communication which delivers synchronisation acquisition in terms of chip and symbol synchronisation and signal strength measurement (SSM).

It is a further object of the invention to provide synchronisation maintenance in terms of chip synchronisation.

Accordingly there is provided a method and apparatus for data communication in a WLAN network using M-ary Code Keying.

Preferably M-ary Code Keying is used for synchronisation of data communication in the network.

Preferably the synchronisation scheme utilises Supergold Structured Codes for acquisition.

Ideally, the synchronisation scheme also utilises Supergold Structured Codes for maintenance.

Ideally, the synchronisation scheme also utilises Supergold Structured Codes for signal strength measurement.

In one arrangement synchronisation maintenance is achieved using an early-late detector.

In a particularly preferred arrangement, synchronisation signals are derived at the output of a bank of correlators during data detection wherein the incoming sequence stream incorporates Structured Codes as mentioned above. This provides a significant improvement in reliability in synchronisation resulting from an improved signal strength on which to synchronise. This implementation allows for the codes to be used for all aspects of communication reducing circuit complexity and cost as well as component count and possibility for error during fabrication of data communication networks. Furthermore, the data communication method and apparatus are more resilient to noise as a result of implementation after correlation.

In one arrangement, the correlators a grouped as a first group, a second group, a third group and a fourth group.

Preferably, the sum of the responses of all correlators in groups to the repetitive periodic transmission of one code, is a constant.

Preferably, the difference signal defines a periodic bipolar waveform referred to as the chip-synchronisation waveform.

In one arrangement, the difference signal is obtained by the difference between the first and third group less second and fourth group.

In another arrangement, the difference signal is obtained by the difference between the second and fourth group less the first and third group.

In a preferred embodiment, the periodic bipolar chip-synchronisation waveform is a squarewave signal.

Preferably, a symbol detector circuit is used at the correlator outputs deriving substantial signal to noise ratio benefit from the processing gain advantage of spread spectrum.

Preferably, an early-late detector circuit is used at the correlator outputs deriving substantial signal to noise ratio benefit from the processing gain advantage of spread spectrum.

Ideally, the waveform used to maintain synchronisation has a period equaling twice the chip period.

Preferably, the correlator coefficients are configured such that when one sample is taken per chip with all signals and correlations taken to be in bipolar form then the sum of the responses of all correlators to the repetitive periodic transmission of one code, is a constant

Ideally also the difference signal is a periodic bipolar waveform with a period equaling twice the chip period. Both of these properties being particularly useful for synchronisation acquisition purposes. Preferably, the difference signal is a squarewave signal.

Ideally, both the method and apparatus described above are formed for both acquisition and maintenance of synchronisation.

Ideally, a transceiver of the system is formed that implements the concept of acquire-and-maintain.

Preferably the symbol acquisition circuitry will deliver a periodic *squarewave* with a periodicity equaling the symbol period.

Ideally, the *squarewave* rising edge coincides with the *symbol* sample at the correlator outputs.

14. According to another aspect of the invention there is provided a method for data communication in a Wireless local area network (WLAN) using a plurality of correlators and M-ary Code Keying with an associated chip period characterised in that the communication utilises a Supergold signature sequence for simultaneously generating:-

a periodic signal for acquiring symbol synchronisation; and

a difference squarewave signal for acquiring and maintaining chip synchronisation.

Preferably, the utilisation of the Supergold signature sequence further generates a sum signal for determining received signal strength and setting threshold levels.

Ideally, the responses of all correlators to the repetitive periodic transmission of one code is a constant.

Preferably, the difference signal is a periodic bipolar squarewave signal.

Ideally, the periodic bipolar squarewave signal has a period of twice the chip period.

In one arrangement, the method utilizes periodic transmission means for producing a zero value sidelobe of a summed correlation.

Preferably, correlator summation is initiated in response to the periodic transmission.

Preferably, the correlator summation is directed to a thresholding circuit.

In one embodiment, the correlator summation is directed to a comparison logic for level determination.

In a particularly preferred embodiment, an early-late detector circuit is connected at the correlator outputs.

Preferably, the method incorporating means for window-thresholding a chip synchronisation waveform.

According to a further aspect of the invention there is provided a data communications apparatus for use in a Wireless local area network (WLAN) incorporating a plurality of correlators and being formed for M-ary Code Keying at an associated chip period characterised in that the apparatus is formed for communication with a Supergold signature sequence to simultaneously generate:-

a periodic signal for acquiring symbol synchronisation; and

a difference squarewave signal for acquiring and maintaining chip synchronisation.

Preferably, the apparatus incorporates means for generating a sum signal for determining received signal strength and setting threshold levels.

Preferably, the sum of the responses of all correlators to the repetitive periodic transmission of one code is a constant.

Ideally, the difference signal is a periodic bipolar squarewave signal.

Preferably, the periodic bipolar squarewave signal has a period of twice the chip period.

In one arrangement, the apparatus incorporates periodic transmission means for producing a zero value sidelobe of a summed correlation.

Preferably, correlator summation is initiated in response to the periodic transmission.

Preferably, the correlator summation is directed to a thresholding circuit.

In one arrangement, the correlator summation is directed to a comparison logic for level determination.

Ideally, an early-late detector circuit is connected at the correlator outputs.

Preferably, the apparatus incorporates means for window-thresholding a chip synchronisation waveform.

The invention will now be described more particularly with reference to the accompanying drawings, which show, by way of example only, one embodiment of data communication method and apparatus according to the invention. In the drawings:

Figure 1 shows a codebook used in the synchronisation scheme of the invention;
Figure 2 shows a bank of correlators for use in the invention;
Figure 3 shows a tapped delay line correlator;
Figure 4 shows Corr(S_0) and Corr(S_2) output waveforms in response to symbol S_0;
Figure 5 shows the Sum(0,2) waveform in response to symbol S_0;
Figure 6 shows the symbol synchronisation waveform generator;
Figure 7 shows symbol synchronisation waveforms;
Figure 8 shows a Harris type early-late detector;
Figure 9 shows the chip synchronisation waveform;
Figure 10 shows the early-late waveform conditions for Supergold encoding;
Figure 11 shows the Supergold early-late detector

For the purposes of this specification reference will be made to the codebook of Figure 1 used in the synchronisation method and apparatus of the invention. The codebook is used to set each of the coefficients of a bank of correlators for use in the invention shown in Figure 2. The bank of correlators shown in Figure 2 is used as part of the maximum likelihood detection process associated with an M-ary Code Keying scheme. In such a detection scheme an incoming symbol is correlated with each sequence in the codebook and the peak correlation value, as determined by a greatest peak detector, identifies the symbol (i.e. sequence) transmitted. The data represented by this symbol can then be recovered accordingly. The essence of this invention is that the properties of Supergold

Structured Codes allow the same bank of correlators, as used in the M-ary detection of data, to be simultaneously used for the acquisition and maintenance of synchronisation.

Defining:-

A as the sum of the responses of a first group of correlators $Corr(S_0)$ to $Corr(S_3)$;
B as the sum of the responses of a second group of correlators $Corr(S_4)$ to $Corr(S_7)$;
C as the sum of the responses of a third group of correlators $Corr(S_8)$ to $Corr(S_{11})$; and
D as the sum of the responses of a fourth group of correlators $Corr(S_{12})$ to $Corr(S_{15})$.

The specific properties being exploited are: (1) that the Sum(0,2) provides an ideal periodic signal from which to acquire symbol synchronisation; (2) the difference signal (A+C)-(B+D) or (B+D)-(A+C) provides an ideal squarewave signal from which to acquire and maintain chip synchronisation; and (3) the sum signal A+B+C+D provides an accurate measure of the received signal strength which can be used to set threshold levels within the synchronisation scheme. It is the unique way in which Supergold encoding provides these signals that constitute the invention within this field.

For convention, the first code, S_0, is selected for periodic application to the input of the bank of correlators. The individual responses of the correlators $Corr(S_0)$ and $Corr(S_2)$ to the application of symbol S_0 are shown below together with the Sum(0,2) = $Corr(S_0)$ + $Corr(S_2)$.

$Corr(S_0)$	16	0	-4	0	0	0	4	0	0	0	4	0	0	0	-4	0
$Corr(S_2)$	0	0	4	0	0	0	-4	0	16	0	-4	0	0	0	4	0
Sum(0,2)	16	0	0	0	0	0	0	0	16	0	0	0	0	0	0	0

The sum of the response of the 0^{th} and 2^{nd} correlators, denoted by Sum(0,2) (for the purposes of this specification the convention Sum(i,j) will be used to denote the summation of the i^{th} and j^{th} correlator outputs), is an ideal impulse occurring at twice the symbol rate. Without loss of generality codes other than S_0 may be used with the correlator combinations being chosen accordingly to give the desired response.

In addition use of the codebook in setting correlator coefficients in this way ensures that, providing at least one sample is taken per chip with all signals and correlations taken to be in bipolar form that:-

the sum of the responses of all correlators to the repetitive periodic transmission of one code, is a constant; and

the difference signal (A+C)-(B+D) or (B+D)-(A+C) is a periodic bipolar squarewave signal with a period equaling twice the chip period.

Both of these properties being particularly useful for synchronisation acquisition purposes.

There are two elements to synchronisation in data communication, irrespective of data type, namely, the acquisition and maintenance of synchronisation.

Acquisition is carried out at the start of data transmission and its sole purpose is to acquire the incoming signal by aligning the receiver chip and symbol clocks with the incoming signal.

Maintenance techniques are used to maintain the chip and symbol clocks in line with the incoming signal during the transmission of the data.

For chip synchronisation to be possible, two samples per chip are needed, thereby doubling the sampling rate. Thus the delay line is designed to have double the length of the correlator (i.e. 32 delay taps instead of just 16). From a detection point of view, the number of taps, however, may be kept at 16, where in this case, a tap is drawn from every other position in the delay-line. The correlator design is shown in more detail in Figure 3.

A perfect periodic impulse being obtained from the sum of the 0^{th} and the 2^{nd} correlator outputs while transmitting code S_0 periodically ensures that the resultant sidelobe of the summed correlation is zero because of the relationship between code S_0 and code S_2. This is also true for codes S_4, S_6, S_8, S_{10} etc. The signal generated is called the symbol-

synchronisation waveform. The symbol-synchronisation waveform contains two peaks marking the start and mid point of a symbol period. In order to remove the ambiguity between which peak marks the start and which peak marks the middle of a symbol period, the individual Corr(S_0) and Corr(S_2) waveforms are compared at the peak instances. At a peak instance when Corr(S_0) exceeds Corr(S_2) then the peak represents the start of the symbol period and when Corr(S_2) exceeds Corr(S_0) then the peak represents the mid point of the symbol period. The occurrence of a peak is determined by threshold detecting the symbol-synchronisation waveform with a threshold set at SSM/2 (i.e. 8 for the length 16 codes used in this example).

Figure 5 shows the summing of Corr(S_0) and Corr(S_2) in response to the periodic transmission of code S_0. Figure 6 shows the implementation of the symbol synchronisation acquisition scheme, where it is assumed that code S_0 is periodically transmitted. The summation of correlators Corr(S_0) and Corr(S_2) is used as an input to a thresholding circuit, which uses a pre-specified threshold of value SSM/2. The outputs of the correlators of interest are also applied to a comparison logic which, when strobed, determines if the output of Corr(S_0) is greater than Corr(S_2) or vise versa.

Every time Sum(0,2) crosses the threshold, a comparison is made between the output Corr(S_0) and Corr(S_2). If the output of Corr(S_0) is greater than Corr(S_2), then a symbol synchronisation is declared by driving the output of the comparison logic high. When the output of Corr(S_2) is greater than Corr(S_0), then the output of the comparison logic is driven low. In this way a symbol clock is generated whose rising edge corresponds to the symbol sample time when the outputs from the correlators are passed to the greatest peak detector for the purpose of data detection.

The upper waveform in Figure 7 constitutes the Sum(0,2), which is applied to the thresholding circuit. After the thresholding and comparison, the output obtained from the comparison circuitry is shown as the lower waveform in Figure 7. It can clearly be seen that the symbol acquisition circuitry of Figure 6 will deliver an ideal periodic *squarewave* with a periodicity equaling the symbol period. Moreover, the rising edge of the *squarewave* coincides with the *symbol* sample in the upper waveform.

During the acquisition phase, symbol synchronisation is usually declared with a high degree of certainty after the successful detection of several contiguous symbols. Once symbol synchronisation has been acquired then a packet based transmission scheme would normally latch the current threshold value, align the symbol clock with the symbol sample time and then rely on chip synchronisation to maintain accurate symbol synchronisation during the transmission of data.

The Harris chip set (described in brief above) takes two samples per chip. Ideally, a sample is required to be placed in the middle of one chip and is referred to as an *end* sample. The other sample will fall in the mid point between the *end* samples of the two consecutive chips, i.e. on the chip transition in the case when there is a chip transition. This sample is referred to as a *mid* sample. Chip synchronisation adjustment can only be made when a chip transition occurs and is detected.

When a chip transition takes place then, with two samples per chip the following sample patterns shown in Figure 8 are possible. The two *end* samples shown in the figure are used for correlation, the *mid* and *end* samples are used for synchronisation purposes. The procedure is as follows:

1 Determine if a chip transition has occurred. A chip transition occurs when the two *end* samples have different signs. The chip transition flag is set.
2 If chip transition occurs then determine if a chip synchronisation error occurred. This is done by comparing the sign of the *mid* sample with the signs of the two *end* samples.
3 If the sign of the *mid* sample is the same as the LHS *end* sample, then sampling is slowed down (i.e. the late flag is set). Else sampling is speeded up (i.e. the early flag is set).

Note this technique will always make a synchronisation adjustment when there is a chip transition. The logic required for the Harris chip tracking is also shown in Figure 8.

Three outputs are produced. The chip transition flag (F) indicates that chip synchronisation information is available when driven to logic '1'. When set, the early (E) and late (L) flags indicate that the receiver sampling clock is running either slow or fast, respectively.

The difference signal (A+C)-(B+D) or (B+D)-(A+C) is a periodic squarewave signal with a period equaling twice the chip period. This is the case when the sampling is perfect, i.e. one sample lies in the middle of the chip while the other lies on a chip transition. Figure 9 depicts this case. The advantage of this waveform is that a transition occurs every chip period and not just every chip transitions.

The effect of early, perfect and late signalling on the resultant periodic squarewave signal is given in Figure 10. While sampling is perfect, samples fall at the maximum (+16) and the minimum (-16), whilst other samples fall exactly at the middle point between the two waveform extremes indicating that a circuit based on the Harris type early-late detector can be used, this circuit is used at the correlator outputs and therefore, derives substantial signal to noise ratio benefit associated with the processing gain advantage of spread spectrum.

Figure 11 shows a modified version of the Harris type early-late detector of Figure 8. The modification is required because it is necessary to window-threshold the chip synchronisation waveform which is no longer binary in general for the arbitrary transmission of symbols.

The modified early-late detector must operate correctly during the phase when the preamble is being transmitted and during the phase when data is being transmitted. During the former the symbol S_0 is transmitted giving the ideal chip-synchronisation waveform shown in Figure 9. For this case a single threshold value of zero may be applied to the chip-synchronisation waveform in order to detect the early and late condition. However, when random data is transmitted the chip synchronisation waveform is no longer an ideal squarewave but instead consists of a number of intermediate discrete values between ±8 (i.e. between ±SSM/2) . By applying a window-threshold of ±8 (i.e. ±SSM/2) to the chip-synchronisation signal produces an unambiguous early-late signal. Though the frequency

of occurrence of the early-late signal is reduced compared to the preamble phase, it occurs frequently enough to maintain chip synchronisation.

The operation of the modified early-late detector illustrated in Figure 11 may be explained by the following truth table.

Samples of Chip-Synchronisation Waveform	Threshold Outputs	Early Flag	Late Flag
16 16 -16	1 1 0	0	1
-16 -16 16	0 0 1	0	1
16 -16 -16	1 0 0	1	0
-16 16 16	0 1 1	1	0
Else	Not Defined	0	0

In the above table *Else* refers to any other condition including the perfect synchronisation conditions {16, 0,-16} and {-16, 0, 16}.

Three samples of the chip-synchronisation waveform are loaded into the 3 tap delay line and the contents of each tap is threshold detected against the window threshold ±T, where T = SSM/2 = 8 for the example given. The binary outputs from the window-threshold detector are fed to the logic device which applies the truth table shown above in order to determine early-late signals. Early-late signals are only produced for the threshold output combinations given in the truth table. Any other combination of threshold outputs including the perfect synchronisation condition as well as exception conditions return no early-late flags indicating that no adjustment of the receiver's clock needs to be made. For the notation adopted, when a late flag is received the receiver clock should be slowed down and when an early flag is received then the receiver clock should be speeded up. In this way chip synchronisation is maintained at the receiver. The 3 tap delay line is updated every chip period in order to ensure that the *mid* sample is always located in the centre tap while the two *end* samples are located in the first and third taps.

In the above description the notation adopted to denote early-late detection is based on the premise that the transmitter clock is fluctuating with respect to the receiver clock. Therefore, when the transmitter clock transition is late then the late flag goes high indicating that the receiver clock should be slowed down. Conversely, when the transmitter clock transition is early then the early flag goes high indicating that the receiver clock should be speeded up.

It is important to note that the Harris type early-late detector illustrated in Figure 8 derives its chip synchronisation signal directly from the received input symbol prior to correlation, that is to say at chip level. For this reason, such detectors specify that a *positive* signal-to-noise ratio is required within the chip bandwidth limiting the proposed solution. In contrast, the technique of the invention is implemented after correlation and does not require this restriction on the SNR ratio in the chip bandwidth, and thus has a broader dynamic SNR range of operation.

During the symbol synchronisation acquisition phase, the sum of the responses of all the correlators (see above) was indicated as being constant at SSM = +16. This constant value constitutes an instantaneous measure of the received signal strength and can be used to derive any signal-strength dependant threshold that is used in the receiver, e.g. the threshold required by both symbol and chip synchronisation procedures.

This signal strength measurement continues to give the required results when the two samples per chip are taken with the correlators as shown in Figure 3. Furthermore, it is also valid under all perfect and imperfect chip synchronisation conditions. However due to the presence of additive noise, it is recommended to average the instantaneous SSM over a number of symbols. This is done during the symbol synchronisation acquisition phase. Once symbol synchronisation is acquired the SSM, and hence the threshold values, can be latched for the duration of the data detection phase. This procedure assumes that there is no change in the signal strength during the transmission of a packet of data.

Once the acquisition phase is completed, the receiver then switches to data receiving mode. During this phase, the receiver must remain in synchronisation in order for optimum data detection to be possible.

The exact symbol sampling instance having been determined from the symbol acquisition phase of the transmission, is used to synchronise the receiver symbol clock. The receiver symbol clock is typically a free running clock with a cycle time of 32 samples. After counting 32 samples the positive edge of this clock is used to latch correlator outputs into the data decision circuit and hence produce received estimates of the transmitted data. When symbol synchronisation is declared the symbol clock is reset. Then one complete symbol can be assumed to be resident in the bank of correlators whenever the counter reaches a count of 32 samples. By maintaining chip synchronisation, the periodicity of the symbol clock remains sufficiently accurate for the correct detection of data.

It will be understood that the current invention relates both to the specific architectures described as embodiments of the underlying invention namely the use of communication codes for synchronisation. This use has the technical effect of reducing component count, complexity and cost. Additionally the manner of use of the signal downstream of the correlators to improve signal quality and therefore system robustness is also an important feature of the invention. Both of the above being read in conjunction with benefits of using Supergold Structured Codes for this purpose.

It will also be understood that the method and apparatus described may be used in any suitable communication medium

It will be noted that the method and apparatus is not limited to implementation with the packet based IEEE 802.11 standard but may equally be implemented with any packet based transmission scheme as well as for synchronous transmission with embedded synchronisation symbols.

It will of course be understood that the present invention is not limited to the specific details described herein, which are given by way of example only and that various modifications and alterations are possible within the scope of the invention.

Claims

1. A method for data communication in a Wireless local area network (WLAN) using a plurality of correlators and M-ary Code Keying with an associated chip period characterised in that the communication utilises a Supergold signature sequence for simultaneously generating:-

    a periodic signal for acquiring symbol synchronisation; and

    a difference squarewave signal for acquiring and maintaining chip synchronisation.

2. A method as claimed in claim 1 in which the utilisation of the Supergold signature sequence further generates a sum signal for determining received signal strength and setting threshold levels.

3. A method as claimed in claim 1 or 2 in which the sum of the responses of all correlators to the repetitive periodic transmission of one code is a constant.

4. A method as claimed in any preceding claim in which the difference signal is a periodic bipolar squarewave signal.

5. A method as claimed in claim 4 in which the periodic bipolar squarewave signal has a period of twice the chip period.

6. A method as claimed in any preceding claim incorporating periodic transmission means for producing a zero value sidelobe of a summed correlation.

7. A method as claimed in claim 6 in which correlator summation is initiated in response to the periodic transmission.

8. A method as claimed in claim 7 in which the correlator summation is directed to a thresholding circuit.

9. A method as claimed in claim 7 or claim 8 in which the correlator summation is directed to a comparison logic for level determination.

10. A method as claimed in any preceding claim in which an early-late detector circuit is connected at the correlator outputs.

11. A method as claimed in claim 10 incorporating means for window-thresholding a chip synchronisation waveform.

12. A data communications apparatus for use in a Wireless local area network (WLAN) incorporating a plurality of correlators and being formed for M-ary Code Keying at an associated chip period characterised in that the apparatus is formed for communication with a Supergold signature sequence to simultaneously generate:-

a periodic signal for acquiring symbol synchronisation; and

a difference squarewave signal for acquiring and maintaining chip synchronisation.

13. An apparatus as claimed in claim 12 incorporating means for generating a sum signal for determining received signal strength and setting threshold levels.

14. An apparatus as claimed in claim 12 or 13 in which the sum of the responses of all correlators to the repetitive periodic transmission of one code is a constant.

15. An apparatus as claimed in any of claims 12 to 14 in which the difference signal is a periodic bipolar squarewave signal.

16. An apparatus as claimed in claim 15 in which the periodic bipolar squarewave signal has a period of twice the chip period.

17. An apparatus as claimed in any of claims 12 to 16 incorporating periodic transmission means for producing a zero value sidelobe of a summed correlation.

18. An apparatus as claimed in claim 17 in which correlator summation is initiated in response to the periodic transmission.

19. An apparatus as claimed in claim 18 in which the correlator summation is directed to a thresholding circuit.

20. An apparatus as claimed in claim 18 or claim 19 in which the correlator summation is directed to a comparison logic for level determination.

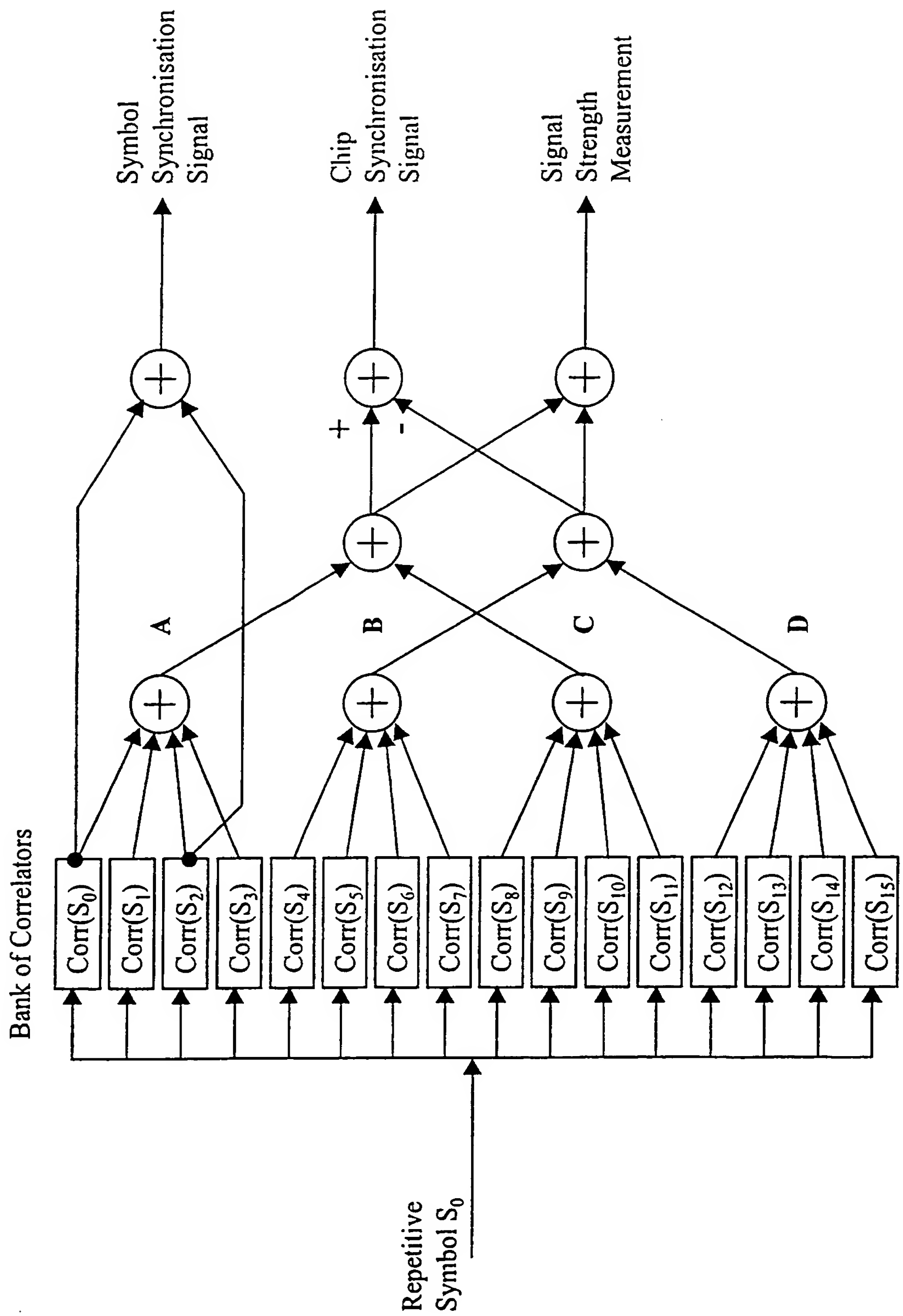
21. An apparatus as claimed in any of claims 12 to 20 in which an early-late detector circuit is connected at the correlator outputs.

22. An apparatus as claimed in claim 21 incorporating means for window-thresholding a chip synchronisation waveform.

Figure 1

Symbol Number	Symbol
S_0	+++-++-++-+++---
S_1	++-++++-+---+-++
S_2	+-+++---+++-++-+
S_3	+---+-++++-++++-
S_4	+++-++-+-+---+++
S_5	++-++++--+++-+--
S_6	-+---++++++-++-+
S_7	-+++-+--++-++++-
S_8	+++---+-+-++-+++
S_9	--+-+++--++++-++
S_{10}	+-++-++++++---+-
S_{11}	-++++-++--+-+++-
S_{12}	---+++-++-++-+++
S_{13}	++-+---+-++++-++
S_{14}	+-++-+++---+++-+
S_{15}	-++++-++++-+---+

Figure 2


Bank of Correlators
Corr(S0)
Corr(S1)
Corr(S2)
Corr(S3)
Corr(S4)
Corr(S5)
Corr(S6)
Corr(S7)
Corr(S8)
Corr(S9)
Corr(S10)
Corr(S11)
Corr(S12)
Corr(S13)
Corr(S14)
Corr(S15)
A
B
C
D
+
-
Symbol Synchronisation Signal
Chip Synchronisation Signal
Signal Strength Measurement
Repetitive Symbol S0

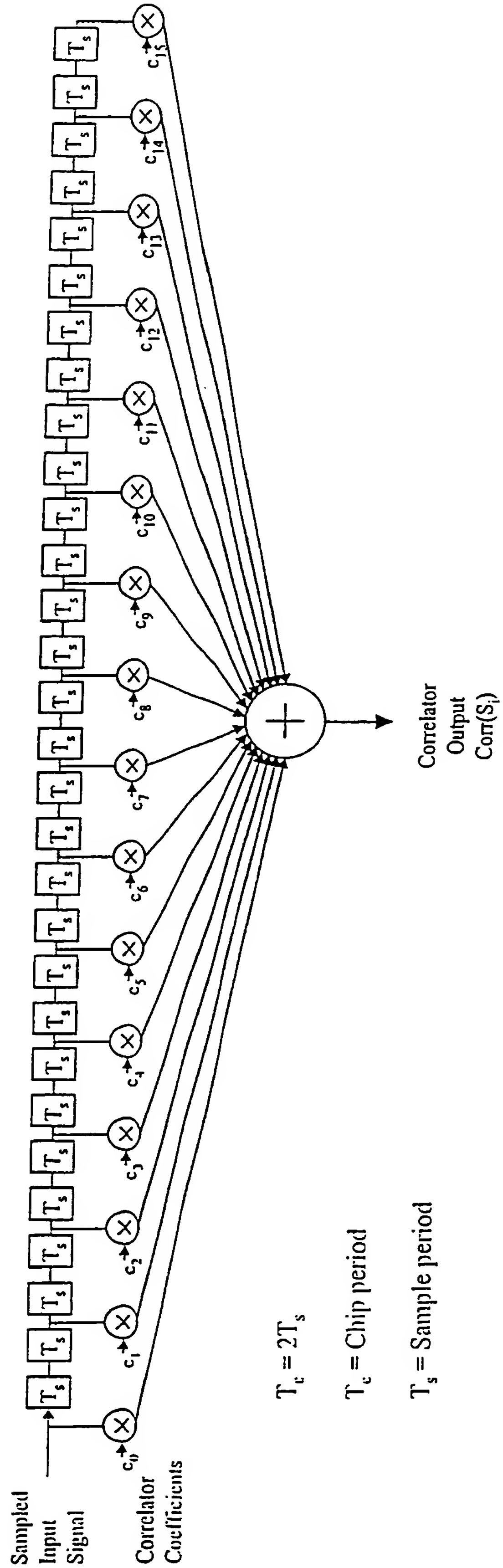

Sampled Input Signal
Correlator Coefficients
T_s
c_0 c_1 c_2 c_3 c_4 c_5 c_6 c_7 c_8 c_9 c_{10} c_{11} c_{12} c_{13} c_{14} c_{15}
Correlator Output Corr(S_i)
$T_c = 2T_s$
T_c = Chip period
T_s = Sample period

Figure 3

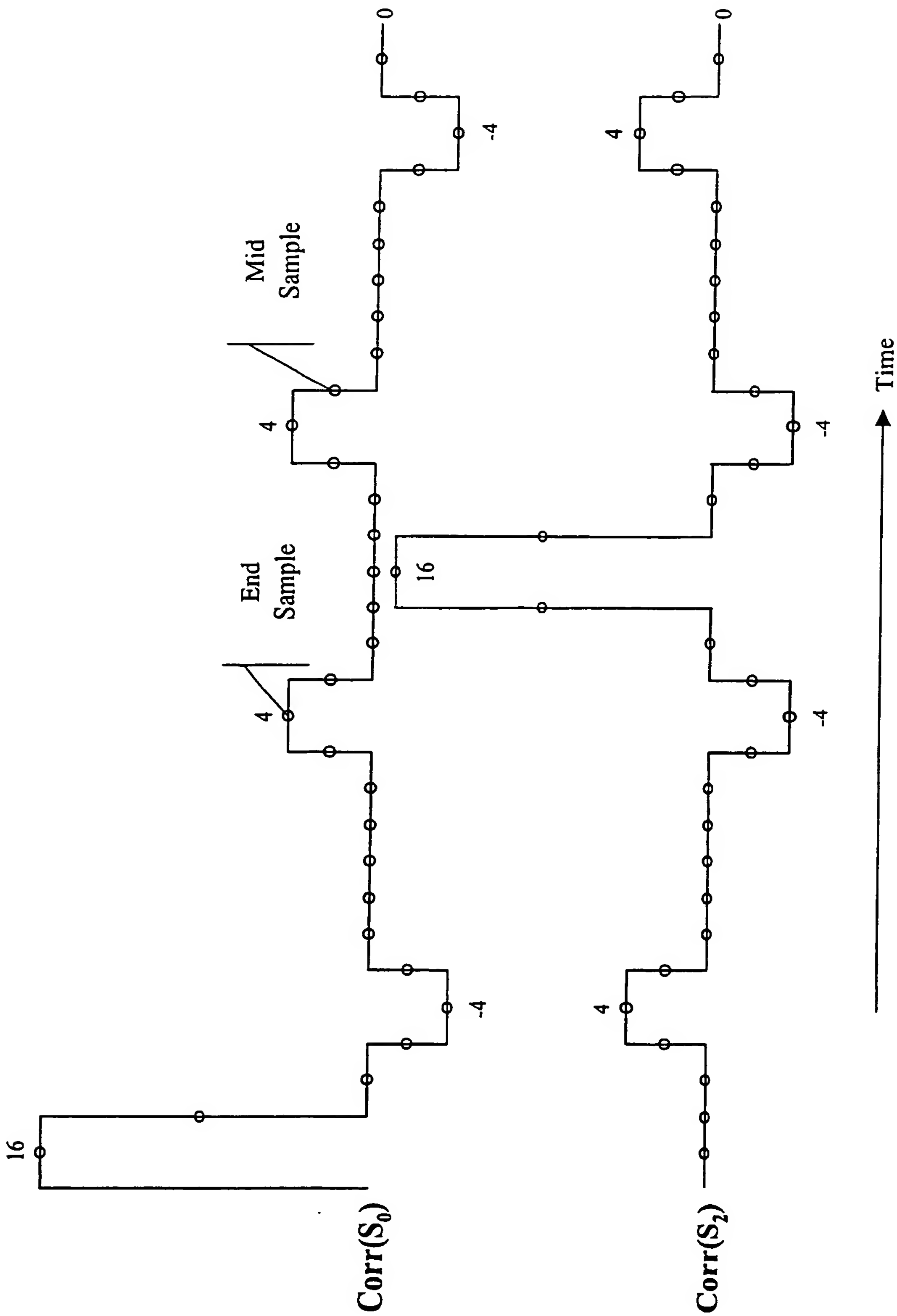
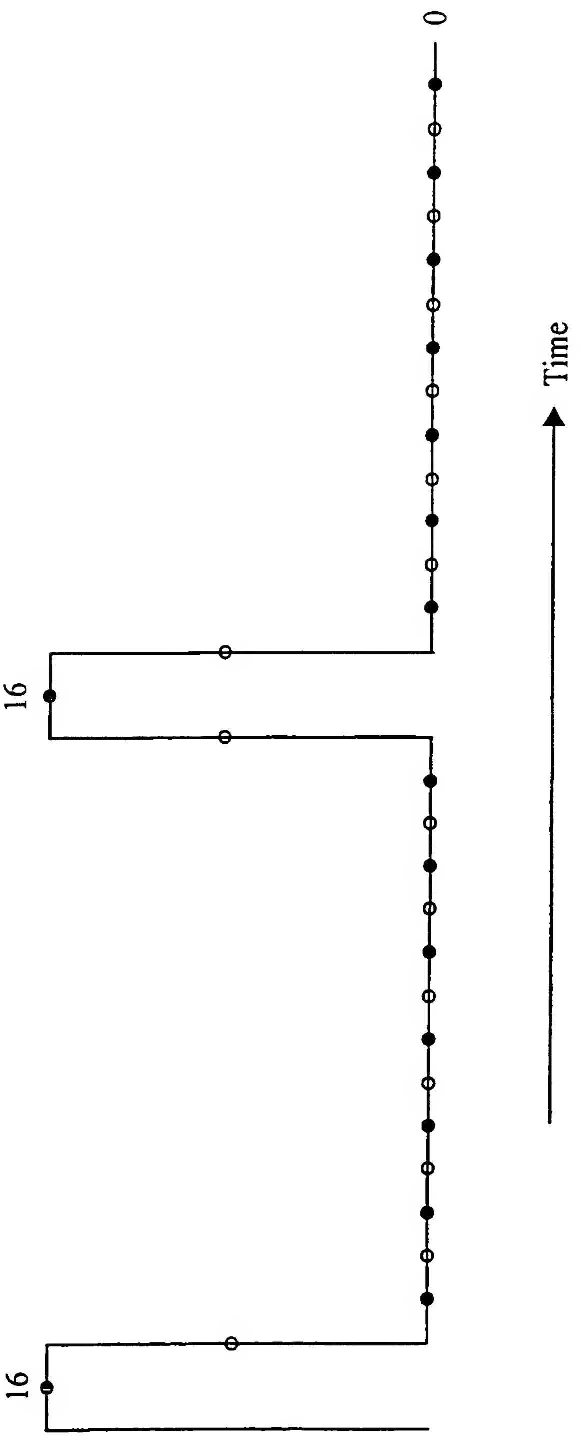


Figure 4



$\mathrm{Sum}(0,2) = \mathrm{Corr}(S_0) + \mathrm{Corr}(S_2)$

Figure 5

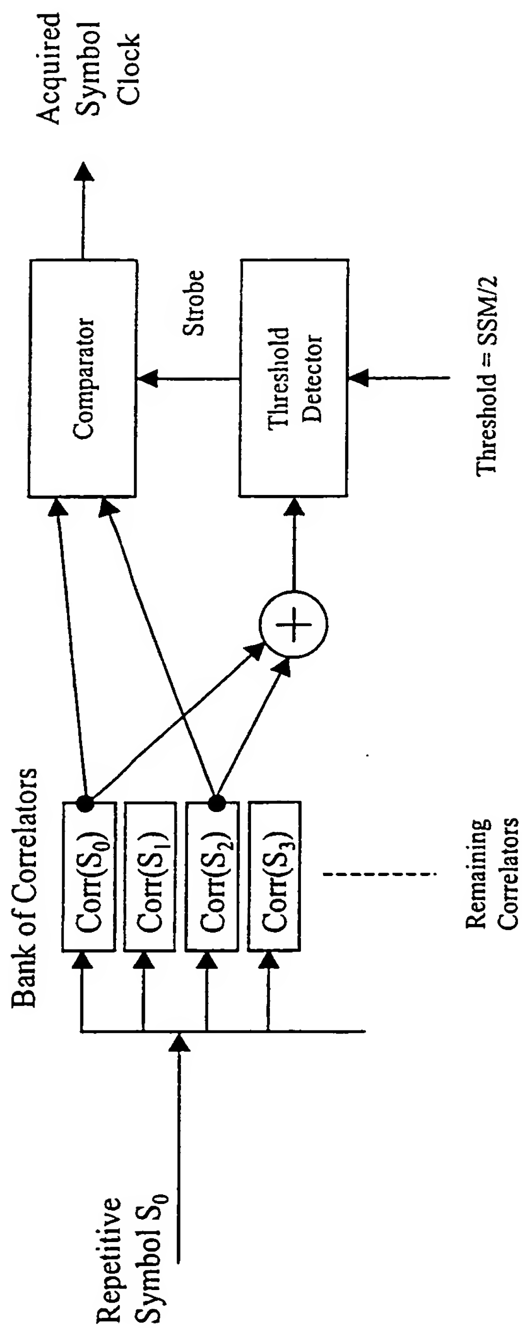

Acquired Symbol Clock
Comparator
Strobe
Threshold Detector
Threshold = SSM/2
Bank of Correlators
Corr(S_0)
Corr(S_1)
Corr(S_2)
Corr(S_3)
Remaining Correlators
Repetitive Symbol S_0

Figure 6

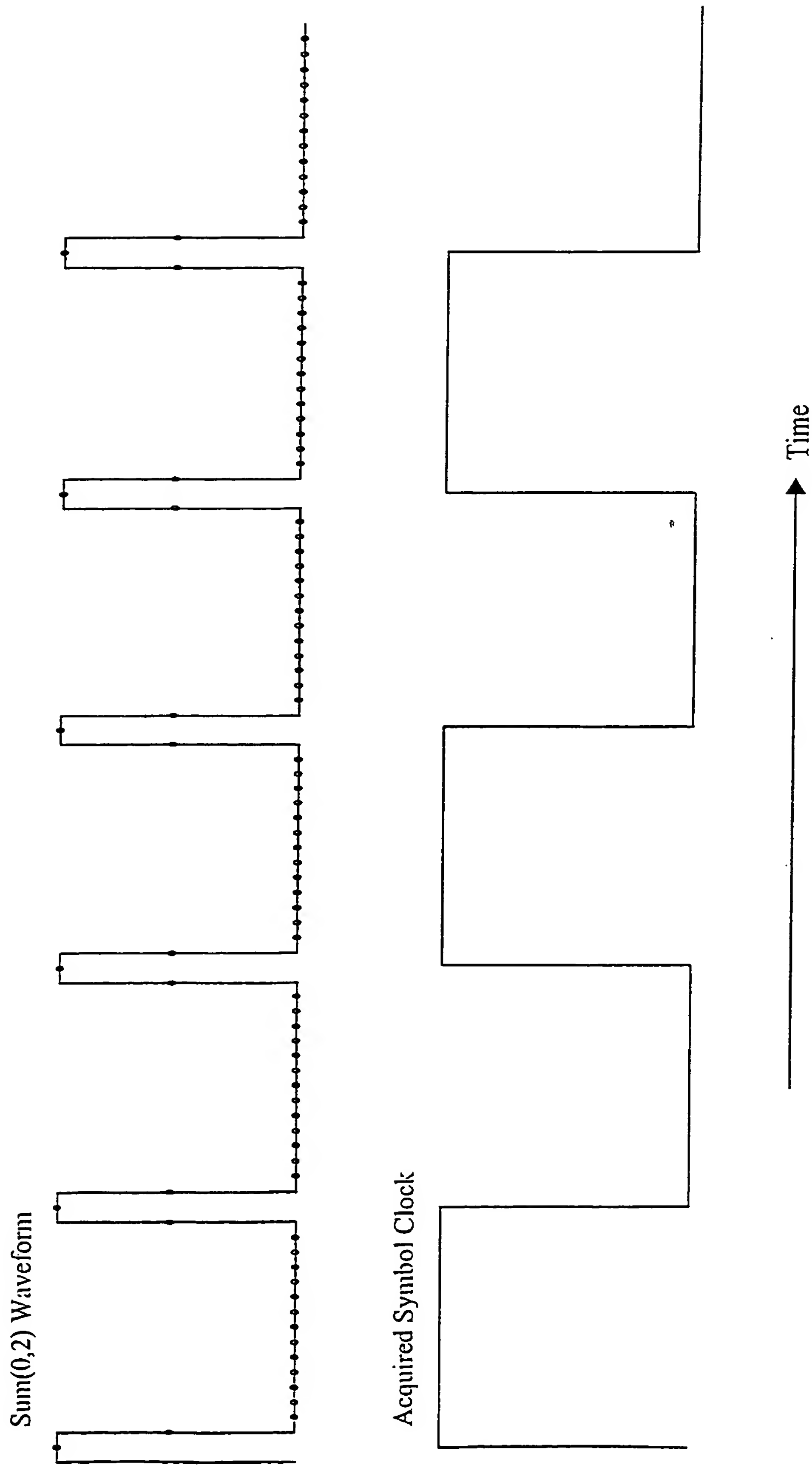


Figure 7

Figure 8

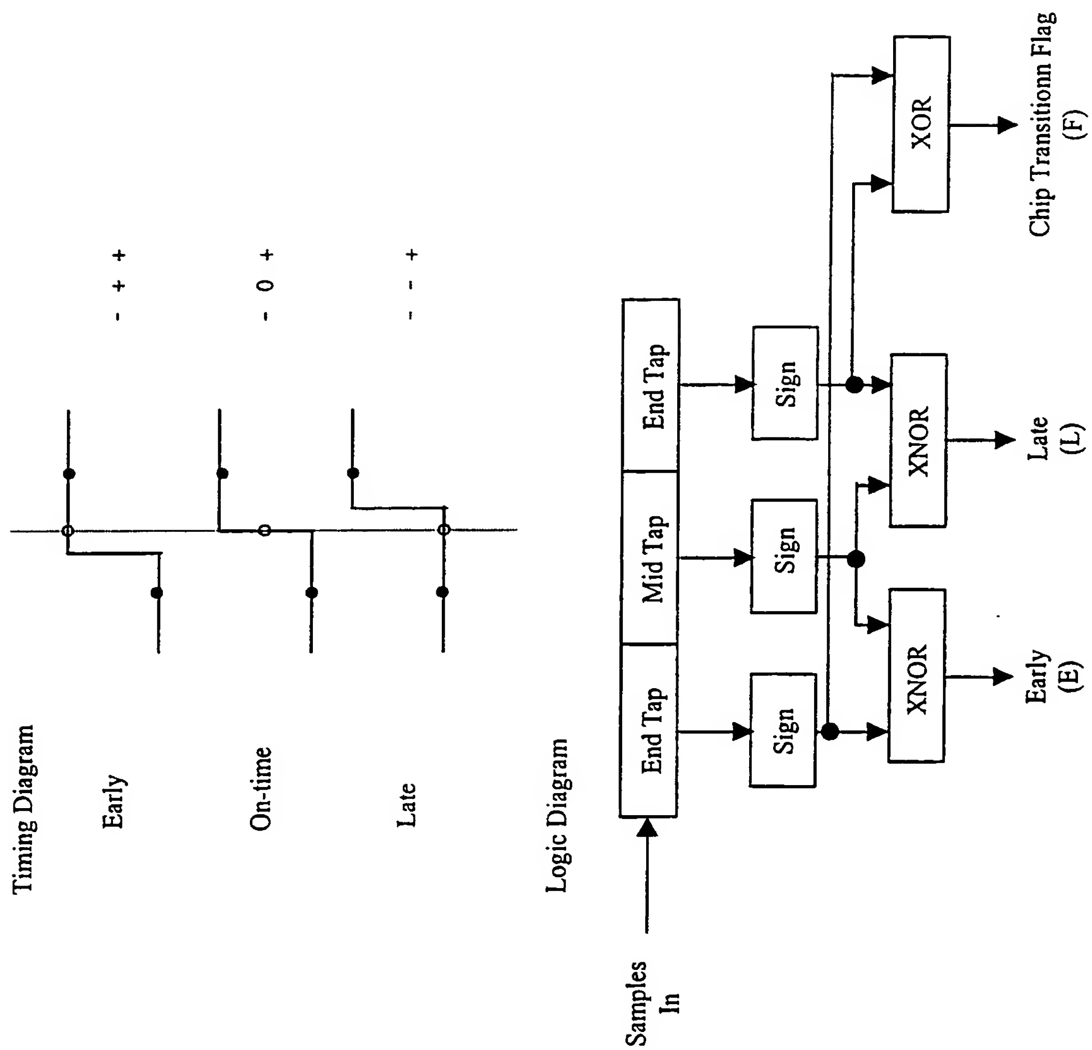
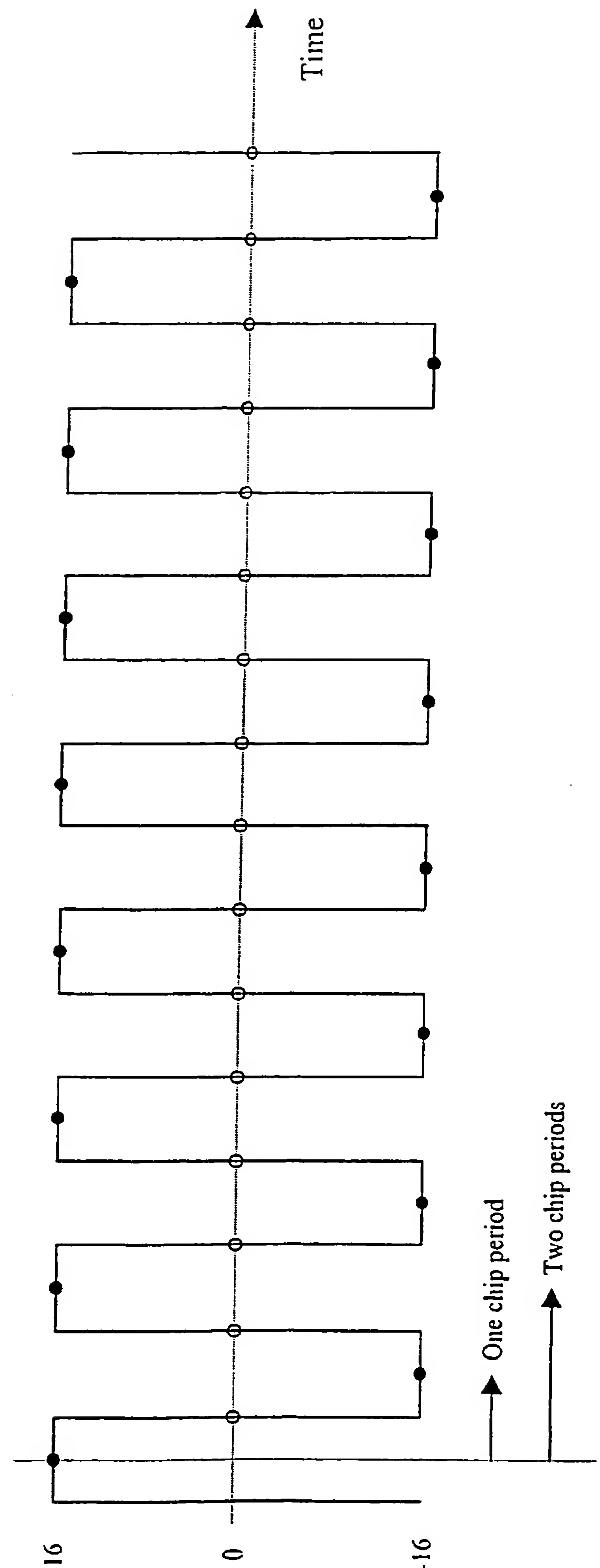

Timing Diagram
Early
- + +
On-time
- 0 +
Late
- - +
Logic Diagram
Samples In
End Tap
Mid Tap
End Tap
Sign
Sign
Sign
XNOR
XNOR
XOR
Early (E)
Late (L)
Chip Transitionn Flag (F)

Figure 9



Ideal Chip Synchronisation Signal

Figure 10

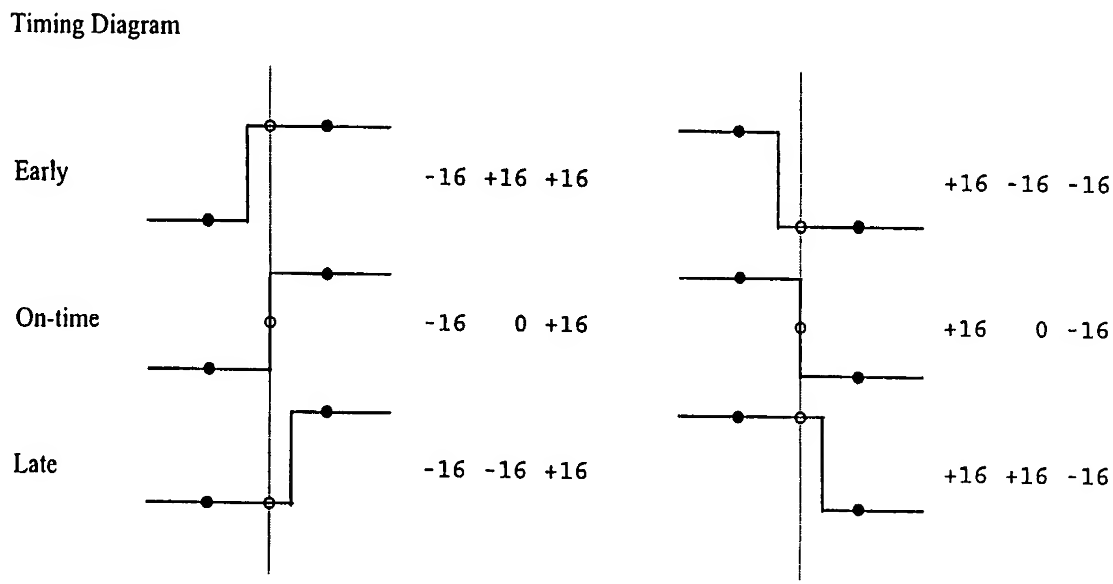
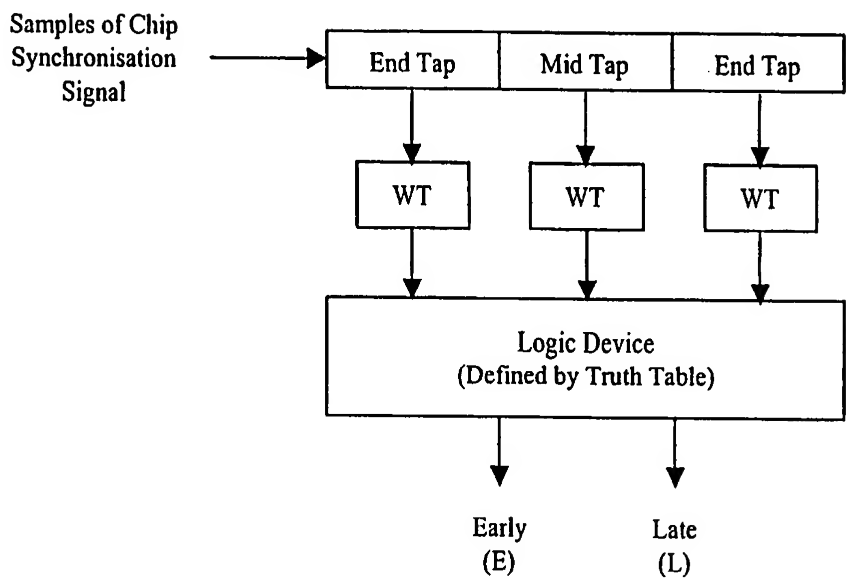

Timing Diagram
Early
-16 +16 +16
+16 -16 -16
On-time
-16 0 +16
+16 0 -16
Late
-16 -16 +16
+16 +16 -16

Figure 11



WT = Window Threshold = ±SSM/2

Else = Any other signal condition

Not Defined = Tri-state logic output

None defined outputs from the WT are discarded by the logic device which returns zeros for both the early and late flags.

Truth Table

Samples of Chip-Synchronisation Waveform	Threshold Outputs	Early Flag	Late Flag
16 16 -16	1 1 0	0	1
-16 -16 16	0 0 1	0	1
16 -16 -16	1 0 0	1	0
-16 16 16	0 1 1	1	0
Else	Not Defined	0	0

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	FOR FURTHER ACTION	see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below.
P8017.WO		
International application No. PCT/IB 00/00536	International filing date *(day/month/year)* 27/04/2000	(Earliest) Priority Date *(day/month/year)* 30/04/1999
Applicant SUPERGOLD COMMUNICATION LIMITED et al.		

This International Search Report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This International Search Report consists of a total of 3 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

   a. With regard to the **language**, the international search was carried out on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

      [ ] the international search was carried out on the basis of a translation of the international application furnished to this Authority (Rule 23.1(b)).

   b. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international search was carried out on the basis of the sequence listing :

      [ ] contained in the international application in written form.
      [ ] filed together with the international application in computer readable form.
      [ ] furnished subsequently to this Authority in written form.
      [ ] furnished subsequently to this Authority in computer readble form.
      [ ] the statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
      [ ] the statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished

2. [ ] **Certain claims were found unsearchable** (See Box I).

3. [ ] **Unity of invention is lacking** (see Box II).

4. With regard to the **title**,

   [ ] the text is approved as submitted by the applicant.
   [X] the text has been established by this Authority to read as follows:

   DATA COMMUNICATION IN A WIRELESS LOCAL AREA NETWORK USING M-ARY CODE KEYING

5. With regard to the **abstract**,

   [X] the text is approved as submitted by the applicant.
   [ ] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. The figure of the **drawings** to be published with the abstract is Figure No. 2

   [X] as suggested by the applicant.
   [ ] because the applicant failed to suggest a figure.
   [ ] because this figure better characterizes the invention.
   [ ] None of the figures.

INTERNATIONAL SEARCH REPORT

International Application No
PCT/IB 00/00536

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04B1/707

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04B H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	ANDREN: "A 2.4 GHz 11 MBps Baseband Processor for 802.11 Applications" HARRIS SEMICONDUCTOR, 'Online! 5 May 1998 (1998-05-05), XP002144808 Retrieved from the Internet: <URL:http://www.intersil.com/prism/papers/baseband.pdf> 'retrieved on 2000-08-11! page 1, right-hand column, line 1 - line 20 page 3, right-hand column, line 32 -page 4, left-hand column, line 5; figure 4 ---	1,12
A	US 5 818 887 A (STEWART KENNETH A ET AL) 6 October 1998 (1998-10-06) column 3, line 55 -column 4, line 16; figure 4 column 6, line 25 - line 50; figure 5 ---	1,12

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
11 August 2000	06/09/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Bossen, M

2

International Application No
PCT/IB 00/00536

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	KOZAKI T ET AL: "A 156-MB/S INTERFACE CMOS LSI FOR ATM SWITCHING SYSTEMS" IEICE TRANSACTIONS ON COMMUNICATIONS,JP,INSTITUTE OF ELECTRONICS INFORMATION AND COMM. ENG. TOKYO, vol. E76-B, no. 6, 1 June 1993 (1993-06-01), pages 684-693, XP000390415 ISSN: 0916-8516 paragraph '02.4!; figure 7 -----	10,21

2

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/IB 00/00536

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5818887 A	06-10-1998	AU 3073497 A	20-02-1998
		CA 2260918 A	05-02-1998
		CN 1229549 A	22-09-1999
		EP 0917778 A	26-05-1999
		WO 9805141 A	05-02-1998

14

REC'D 01 AUG 2001
WIPO PCT

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference P8017.WO	**FOR FURTHER ACTION** See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)	
International application No. PCT/IB00/00536	International filing date *(day/month/year)* 27/04/2000	Priority date *(day/month/year)* 30/04/1999
International Patent Classification (IPC) or national classification and IPC H04B1/707		
Applicant SUPERGOLD COMMUNICATION LIMITED et al.		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 6 sheets, including this cover sheet.

   ☒ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 7 sheets.

3. This report contains indications relating to the following items:

   I ☒ Basis of the report
   II ☐ Priority
   III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   IV ☐ Lack of unity of invention
   V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations suporting such statement
   VI ☐ Certain documents cited
   VII ☐ Certain defects in the international application
   VIII ☒ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
14/11/2000	26.07.2001
Name and mailing address of the international preliminary examining authority: European Patent Office - P.B. 5818 Patentlaan 2 NL-2280 HV Rijswijk - Pays Bas Tel. +31 70 340 - 2040 Tx: 31 651 epo nl Fax: +31 70 340 - 3016	Authorized officer Bossen, M Telephone No. +31 70 340 3592

Form PCT/IPEA/409 (cover sheet) (January 1994)

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/IB00/00536

I. Basis of the report

1. With regard to the **elements** of the international application *(Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17))*:
Description, pages:

3-15	as originally filed	
1,2,16	with telefax of	14/06/2001

Claims, No.:

1-22	with telefax of	14/06/2001

Drawings, sheets:

1/11-11/11	as originally filed

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

   These elements were available or furnished to this Authority in the following language: , which is:

   ☐ the language of a translation furnished for the purposes of the international search (under Rule 23.1(b)).
   ☐ the language of publication of the international application (under Rule 48.3(b)).
   ☐ the language of a translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

   ☐ contained in the international application in written form.
   ☐ filed together with the international application in computer readable form.
   ☐ furnished subsequently to this Authority in written form.
   ☐ furnished subsequently to this Authority in computer readable form.
   ☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
   ☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

- ☐ the description, pages:
- ☐ the claims, Nos.:
- ☐ the drawings, sheets:

5. ☒ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)):

   (Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.)
   see separate sheet

6. Additional observations, if necessary:

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	1-22
	No:	Claims	
Inventive step (IS)	Yes:	Claims	1-22
	No:	Claims	
Industrial applicability (IA)	Yes:	Claims	1-22
	No:	Claims	

2. Citations and explanations
   see separate sheet

VIII. Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:
see separate sheet

<u>Re Item I</u>

Basis of the report

1 The amendments filed with the telefax dated 14.6.2001 introduce subject-matter which extends beyond the content of the application as filed, contrary to Article 34(2)(b) PCT.

2 The amendments concerned are the following:

Page 2, line 34:	reference to document WO-A-9933212
Claim 1 and 12:	introduction of features from WO-A-9933212 in order to specify "Supergold sequences"

3 WO-A-9933212 was published after the priority date of the current application. The man skilled in the art would not have been aware of its existence at that date.

4 Further, it is not unambiguously derivable from the application as originally filed that the codes used in the invention are those defined in WO-A-9933212.

5 The teaching of WO-A-9933212 therefore does not constitute prior art from which material could be introduced into the application to clarify an obscurity. Hence abovementioned amendments are not allowable.

Re Item V

Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

6 The application lacks clarity because the independent claims 1 and 12 are not clear (See also Re Item VIII).

7 Notwithstanding the clarity objection, the subject-matter of the present invention is regarded as being novel and inventive for the following reasons:

8 The process of synchronisation in spread spectrum system in the prior art consists of two steps.

9 First the chip phase has to be found. This step, also called acquisition, is known in the prior art. D1, cited in the description on page 1, line 28-29, shows acquisition.

10 After acquisition the chip phase has to be maintained in order to demodulate the signal. This second step, which is called tracking, is also known in the prior art. D2, cited in the description on page 2, line 9-11, shows tracking using an early-late loop.

11 For the acquisition to reach an acceptable accuracy, the received signal has to be oversampled increasing the component count.
Since the tracking operates directly on the received signal it is known to lead to reliability problems.

12 The method (claim 1) and apparatus (claim 12) of the invention uses structured code sequences for M-ary code keying such that the difference between the sum of even groups of correlator outputs and the sum of odd groups of correlator outputs creates a chip synchronisation signal without further need of acquisition and tracking.

13 None of the documents cited in the search report anticipate or suggest such a use of the correlators.

14 The subject-matter of claims 1 and 12 is therefore considered as involving an inventive step (Article 33(3) PCT).

15 Claims 2-11 being dependent on claim 1 and claims 13-22 being dependent on claim 12 as such also meet the requirements of the PCT with respect to novelty and inventive step.

Re Item VIII

Certain observations on the international application

16 The inclusion of the wording "... a chip synchronisation signal being generated by subtracting the sum of even groups of correlator outputs from the sum of odd groups of correlator outputs." in claim 1 combined with a specification that the signature sequences are structured codes, is believed to define the subject-matter sufficiently for a man skilled in the art to carry out the invention for the following reason:

17 Using a method of trial and error, the man skilled in the art would be able to verify whether a set of structured codes, to be used in the method of the invention, produces the periodic signal for acquiring symbol synchronisation and the chip synchronisation signal, using the method claim 1.

18 Similar observations apply to claim 12.